Notice of Allowability	Application No.	Applicant(s)	
	10/665,931	MOTOKAWA ET AL.	
	Examiner	Art Unit	
	Mark P. Francis	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *05/10/07*.

2. ☒ The allowed claim(s) is/are *1,2,4,5,8-16 and 19*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Examiner's Amendment

1. This Office Action is responsive to the communication filed May 10, 2007.

2. Per applicant's request, amended claims 1,4,8,9, and 19 have been entered.

Claim 7,17, and 18 have been cancelled.

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. Authorization for this examiner's amendment was given by George B. F. Yee, Reg. 37,478 on June 22, 2007.

Listing of Claims:

1. (Currently amended) A compiler for producing an object program from a source program ~~used~~ to be executed on an architecture equipped with a plurality of memory hierarchies ~~from a source program in conjunction with a computer system~~, the compiler configured to operate a computer to perform steps comprising:

a step for detecting ~~interpreting either an option or~~ a designation statement designating which memory hierarchy among the plurality of memory hierarchies will serves as the main data store for an object program ~~a target program mainly refers to data present in,~~ when the ~~target~~ object program is executed; [[and]]

a step for performing an optimizing process directed to said designated memory hierarchy to produce the object program; and

a step for storing the object program on a data store.

2. (Currently amended) A compiler as claimed in claim 1, wherein:

~~as said optimizing process directed to the designated memory hierarchy,~~ a memory latency is calculated according to the designated memory hierarchy with respect to an instruction for accessing a memory location in the designated memory hierarchy; ~~and an~~ wherein said optimizing process ~~responding to~~is based on the calculated latency ~~is carried out~~.

3. (Currently amended) A compiler as claimed in claim 1, wherein:

~~as said optimizing process directed to the designated memory hierarchy,~~ a loop transformation method of a loop interchange, a loop unrolling, or a loop tiling is determined according to the designated memory hierarchy with respect to a memory access instruction; and wherein said optimizing process is based thereon.

4. (Currently amended) An object program producing method executed by both a computer system and a compiler executing on the computer system for producing an object program ~~used~~ to be executed on an architecture equipped with a plurality of memory hierarchies from a source program ~~in conjunction with a computer system~~,

said method comprising:

a step for detecting ~~interpreting either an option or~~ a designation statement designating which memory hierarchy ~~a target~~an object program mainly refers to for storing and accessing data ~~present in,~~ when the ~~target~~ object program is executed; [[and]]

a step for performing an optimizing process directed to said designated memory hierarchy to produce the object program; and

a step for outputting and storing the object program on a data store.

5. (Currently amended) A code producing method as claimed in claim 4, wherein:

[[as]]for said optimizing process directed to the designated memory hierarchy, a memory latency is calculated according to the designated memory hierarchy with respect to a

memory access instruction; and an optimizing process according to the calculated latency is carried out.

6. (Currently amended) A code producing method as claimed in claim 4, wherein:

[[as]]for said optimizing process directed to the designated memory hierarchy, a loop transformation method of a loop interchange, a loop unrolling, or a loop tiling is determined according to the designated memory hierarchy with respect to a memory access instruction.

7. (Canceled)

8. (Currently amended) A storage medium wherein:

said storage medium has stored there into [[the]]a compiler for producing an object program from a source program to be executed on an architecture equipped with a plurality of memory hierarchies, the compiler configured to operate a computer to perform steps comprising:~~recited in claim 1.~~

a step for detecting a designation statement designating which memory hierarchy among the plurality of memory hierarchies will serves as the main data store for an object program when the object program is executed;

a step for performing an optimizing process directed to said designated memory hierarchy to produce the object program; and

a step for storing the object program on a data store.

9. (Currently amended) A method for producing an object program ~~used~~ to be executed on an architecture equipped with a plurality of memory hierarchies from a source program in conjunction with a computer system, wherein:

said computer system executes:

a step for ~~analyzing~~ detecting a designation statement designating which hierarchy an object program mainly refers to for storing data ~~stored in a memory of,~~ when said object program is executed; [[and]]

a step for producing said object program in which an optimizing process including different processes sequences according to said plural memory hierarchies is carried out with respect to said source program~~, and an object program which has been optimized as to an access to said memory hierarchy is produced~~ by selecting a process[[es]] sequence corresponding to the memory hierarchy designated by said designation statement; and

a step for storing the object program on a data storage device.

10. (Original) An object program producing method as claimed in claim 9, wherein:

said designation statement is described in an option within a compiler initiating command.

11. (Original) An object program producing method as claimed in claim 9, wherein:

said designation statement is inserted into said source program.

12. (Original) An object program producing method as claimed in claim 11, wherein:

said designation statement is applied to each of plural loops contained in said source program;

said analysis step includes a step for forming a loop table indicative of a correspondence relationship between the respective loops and the memory hierarchies designated by the designation statements corresponding to said loops; and

said execution step includes a step for acquiring a memory hierarchy designated by said designation statement by referring to said loop table.

13. (Original) An object program producing method as claimed in claim 9, wherein:

said memory hierarchies include a hierarchy constructed of a primary cache, a hierarchy constructed of a secondary cache, and a hierarchy constructed of a main storage apparatus.

14. (Original) An object program producing method as claimed in claim 9, wherein:

said optimizing process contains at least one of an optimizing process by instruction scheduling, a prefetch optimizing process, and an optimizing process by loop tiling and loop interchange/loop unrolling.

15. (Original) An object program producing method as claimed in claim 14, wherein:

said optimizing process corresponds to the optimizing process by the instruction scheduling; and a number of memory access latency cycles to be set are different from each other according to said memory hierarchies in said processes sequence.

16. (Original) An object program producing method as claimed in claim 14, wherein:

said optimizing process corresponds to the prefetch optimizing process; and timing of a prefetch code to be inserted is different from each other according to said memory hierarchies in said processes sequence.

17. (Original) An object program producing method as claimed in claim 14, wherein:

said optimizing process corresponds to the optimizing process by the loop tiling; a tile size is different from each other according to said memory hierarchies in said processes sequence.

18. (Original) An object program producing method as claimed in claim 14, wherein:

said optimizing process corresponds to the optimizing process by the loop interchange/loop unrolling; and in said processes sequence, it is determined to apply, or not to apply either the loop interchange or the loop unrolling according to said memory hierarchies.

19. (Currently amended) An apparatus for producing an object program used to be executed on an architecture equipped with a plurality of memory hierarchies from a source program, comprising:

a storage apparatus for previously storing thereinto an optimizing process containing different process[[es]] sequences according to said plurality of memory hierarchies;

an input apparatus for inputting said source program and a designation statement designating which memory hierarchy an object program mainly refers to data present in, when said object program is executed;

a processing apparatus for producing an optimized object program based upon both said source program and said designation statement; and

an output apparatus for outputting said optimized object program; wherein:

said processing apparatus executes:

a step for analyzing said designation statement;

a step for producing an object program which has been optimized as to an access to said memory hierarchy by selecting a processes sequence corresponding to the memory hierarchy designated by said designation statement; and

a step for outputting said optimized object program ~~form~~ from said output apparatus.

Allowable Subject Matter

5. The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or fairly suggest at least the feature of:

wherein a loop transformation method of a loop interchange, a loop unrolling, or a loop tiling is determined according to the designated memory hierarchy with respect to a memory access instruction, wherein said optimizing process is based thereon as recited in each of the independent claims 1,4,8,9, and 19.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

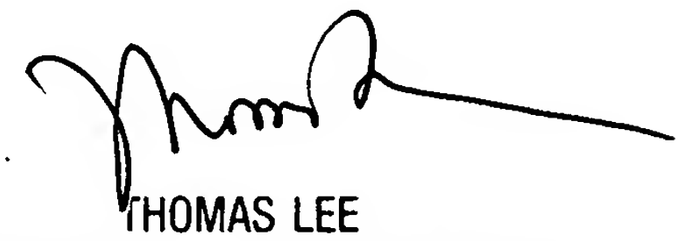
accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark P. Francis whose telephone number is (571)272-7956. The examiner can normally be reached on Mon-Fri 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T.An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100